Docket No.

2312-0866-2PCT

IN RE APPLICATION OF: KIMIHIR MATSU

SERIAL NO: 09/530,588

FILED:

MAY 5, 2000

FOR:

WIRING STRUCTURE OF SEMICONDUCTOR DEVICE, ELECTRODE, AND METHOD FOR FO

THEM

ASSISTANT COMMISSIONER FOR PATENTS WASHINGTON, D.C. 20231

SIR:

Transmitted herewith is an amendment (w/ Marked-Up Copy) in the above-identified application.

- □ No additional fee is required
- □ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.
- Additional documents filed herewith:

Marked-Up Copy, Petition for Extension of Time (1 mo.)

The Fee has been calculated as shown below:

CLAIMS	CLAIMS REMAINING		HIGHEST NUMBER PREVIOUSLY PAID	NO. EXTRA CLAIMS	RATE	CALCULATIONS
TOTAL	46	MINUS	43	3	× \$18 =	\$54.00
INDEPENDENT	6	MINUS	9	0	× \$84 =	\$0.00
INDEFENDENT		☐ MULTIPLE DEPENDENT CLAIMS + \$280 =				\$0.00
			TOTAL OF A		JLATIONS	\$54.00
□ Reduction by 50% for filing by Small Entity					\$0.00	
		Recordation of Assignment + \$40 =			\$0.00	
		- Recon	dation of rissignment		TOTAL	\$54.00

- A check in the amount of \$164.00 is attached.
- Please charge any additional Fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.
- If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time may be charged to Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

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2312-0866-2PCT

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF:

:

3/29/2

KIMIHIRO MATSUSE ET AL

: EXAMINER: QUACH, T.

SERIAL NO: 09/530,588

. 03/220,011

FILED: MAY 5, 2000

: GROUP ART UNIT: 2814

FOR: WIRING STRUCTURE OF

SEMICONDUCTOR DEVICE, ELECTRODE, AND METHOD

FOR FORMING THEM

:

AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS WASHINGTON, D.C. 20231

SIR:

In response to the Official Action dated November 26, 2001, please amend the above-identified application as follows:

IN THE CLAIMS

Please cancel Claims 28-62 without prejudice.

Please add the following new claims.

63. (New) A method of forming a wiring structure of a semiconductor device,

comprising:

forming a first conducting layer by depositing a metal film on an insulating film

formed on a semiconductor substrate;

forming an interlayer insulating film over an entire surface of the semiconductor

substrate so as to cover from above the first conducting layer;

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